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GitHub - ultraembedded/core_ddr3_controller: A DDR3 memory ...

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If you have not already read UG406 and DS186, there is a great deal of helpful information available in these two documents. You cannot connect a single DRAM device to more than one memory controller. From DS186: (DDR3) Multiple controllers per FPGA supported through the Memory Interface Generator (MIG) tool.

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DDR4 Controller | Interface IP - Rambus

Figure 1-1 on page 1-1 shows a system-level diagram including the example top-level file that the DDR3 SDRAM Controller with ALTMEMPHY IP creates for you. The MegaWizard™ Plug-In Manager generates an example top-level file, consisting of an example

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driver, and your DDR3 SDRAM high-performance controller custom variation.

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Double Data Rate (DDR3) SDRAM Controller IP Core
DDR3 Controller. Overview. Documentation.

Overview. The Xilinx DDR3 controller is high performance (2133Mbps in UltraScale) with support for lower power DDR3L as well as UDIMMs, SODIMMs, and RDIMMs.

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